REMARKS

Claims 1, 2, 4-9, 11-15, and 17-20 are presently pending. Claims 3, 10, and 16 are cancelled without prejudice.

Claims 1, 2, 8, and 9 were rejected under 35 U.S.C. § 102(a) as being anticipated by Wise. Claim 1 is amended to recite, among other limitations, "wherein the logic determines whether the parameters received by the input are valid based on the picture type indicator and the number of motion vectors received by the input". Examiner has indicated that Wise does not specifically teach the logic determines whether the parameters received by the input are valid based on the picture type indicator and the number of motion vectors received by the input. Office Action at 3. Accordingly, Assignee respectfully requests that Examiner withdraw the rejection to claims 1 and 2 under 35 U.S.C. § 102(a).

However, Examiner has indicated that "Kim teaches the logic determines whether the parameters received by the input are valid based on the picture type indicator and the number of motion vectors received by the input. [Col. 1 Lines 44-57]." Office Action at 3.

Kim, Col. 1, Lines 44-57 recite:

> A maximum of 4 MVs can be obtained per macroblock, but transmitting the obtained MVs directly may results in a transmission of a substantial number of bits. To reduce the bits for transmission, the difference between MVs of the current and the preceding macroblock is coded VLC and transmitted. The MV value of the preceding macroblock is stored in a MV predictor and is expressed as pmv[r][s][t]. Namely, the pmv value is the MV of the preceding macroblock (MB) and a value to be coded by the encoder is "vector[r][s][t]-pmv[r][s][t]". The parameters "r" for field type, "s" for picture type, and "t"

> for direction of vector typically have values of either 0 or 1 and have meanings as shown in Table 1 below. Also, "DMV" represents a difference between the two MVs.

Assignee respectfully submits that the mere teaching of “A maximum of 4 MVs can be obtained per macroblock” does not teach that the “logic determines whether the parameters received by the input are valid based on the picture type indicator and the number of motion vectors received by the input”. It is first noted that Kim does not even teach even teach determining “whether the parameters received by the input are valid”. Moreover, even if Kim’s statement that “A maximum of 4 MVs can be obtained per macroblock” is construed to determine “whether parameters received by the input are valid” it is not “based on the picture type indicator”. Accordingly, Assignee respectfully traverses the rejection to claim 3 as originally submitted, and requests that Examiner allow claim 1 as now amended, as well as dependent claims 2, and 4-7.

Claim 4 was rejected under 35 U.S.C. § 103(a) as obvious from the combination of Wise and Kim. Claim 4 recites, among other limitations, “a control register for providing the type of pictures and indicating the number of motion vectors received to the logic”. Examiner has indicated that “Wise (modified by Kim) teaches a control register for providing the type of pictures and indicating the number of motion vectors received to the logic. [Wise- Pg. 51 0682 Table A.3.2; Kim - Col. 1 Lines 44-57; Fig. 1; Fig. 4].”

Although, Wise, Pg. 51, Table A.3.2 includes an entry “PICTURE_TYPE MPEG” and Kim, col. 1, line 44 discloses that “A maximum of 4 MVs can be obtained per macroblock”, the

foregoing do not teach “a control register for providing the type of picture and indicating the number of motion vectors received to the logic”. Kim, Figure 1 is “a block diagram of a MV decoder” (Col. 5, Line 41) and Figure 4 “is a detailed block diagram of a MV adder” (Col. 5, Line 47). However, Kim, Figures 1 and 4 do not include anything “for providing the type of picture and indicating the number of motion vectors received to the logic”. Accordingly, Assignee respectfully traverses the rejection to claim 4 and requests that Examiner withdraw it.

Claim 5 was rejected under 35 U.S.C. § 103(a) as being obvious from the combination of Wise in view of Kim. Claim 5 recites, among other limitations, “wherein the control register comprises one or more bits, each of which are associated with a corresponding one or the one or more motion vector registers, wherein the one or more bits are in a particular state, based on whether the corresponding motion vector register stores a motion vector”.

Examiner has indicated that Wise (as modified by Kim) teaches the foregoing, at [Kim – Abstract; col. 1 lines 44-57; Fig. 1; Fig. 4; Fig. 6; Col. 6, Lines 8-12]. Kim, Abstract teaches:

> The motion vector decoder includes a parameter delay block which delays transmissions of various input signals necessary for motion vector decoding; a motion vector residual block which extracts a motion residual value and outputs a positive number of the motion residual value; a motion vector code table block which searches for a motion code, a condition of a sign of the motion code, and a zero condition of the motion code using a variable length decoding table and outputting the searched values; a motion vector delta block which calculates a difference of motion vectors from the motion vector residual

> block and the motion vector code table block; a MV adder which adds the difference value received from the motion vector delta block and a motion vector of a preceding macroblock to output a new motion vector; and a register which updates a flip-flop corresponding to a current (r, s, t) of a new motion vector. The circuit blocks each have at least one flip-flop to allow processing of each block within a single clock.

Although in Kim, Abstract, the "motion vector decoder" includes a number of things, e.g., "a parameter delay block", "a motion vector residual block", "motion vector code table", etc., Kim abstract does not teach anything that "comprises one or more bits, each of which are associated with a corresponding one of the one or more motion vector registers, wherein the one or more bits are in a particular state, based on whether the corresponding motion vector register stores a motion vector".

Moreover, Kim, Col. 6, Lines 8-12 recites that:

> The vlc[10:0], shown in FIG. 2(e), is a MV value variable length coded by the encoder and is received by the MV residual block 11 and the MV code table block. Since maximum of 11 data bits may be produced through the VLC, the vlc[10:0] has a length of 11 bits and is the most significant bit (msb). The msb value may or may not be sent by the encoder and if sent, one or all eight values may be sent.

(Emphasis Added). It is noted that Kim does not tech that "vlc[10:0]" "comprises one or more bits, each of which are associated with a corresponding one of the one or more motion vector registers". Moreover, it is noted that "vlc" appears to have 11 bits, "[10:0]", while also indicating that "A maximum of 4 MVs can be obtained per macroblock" at Col. 1, Line 44. Thus vlc[10:0] does not "comprise[s] one or more bits, each of which are associated with a

corresponding one of the one or more motion vector registers, wherein the one or more bits are in a particular state, based on whether the corresponding motion vector register stores a motion vector". Accordingly, Assignee respectfully traverses the rejection to claim 5 and requests that Examiner withdraw it.

Claim 6 was rejected under 35 U.S.C. § 103(a) as obvious from the combination of Wise in view of Kim. Claim 6 recites, among other limitations, "wherein the logic determines that the parameters are invalid if the control register indicates that the type of picture is an I-picture and any of the one or more bits are in the particular state". Examiner has indicated that the foregoing is taught at Wise-pg. 51 0682 Table A.3.2; Pg. 13, 0160, 0165; pg. 18, 0220-0221; pg. 117 1595; Kim - Abstract; Col. 1 Lines 44-57; Fig. 1; Fig. 4; Fig. 6; Col. 6 Lines 8-12.

For the reasons indicated above, Kim - Abstract; Col. 1 Lines 44-57; Fig. 1; Fig. 4; Fig. 6; Col. 6 Lines 8-12 does not teach the limitations of claims 1 (as now amended), 4 and 5. Furthermore, clearly the foregoing as well as Wise, Pg. 13, 0160, 0165; pg. 18, 0220-0221; pg. 117 1595, do not even mention the conditions "that the type of picture is an I-picture", "any one of the one or more bits are in the particular state". Accordingly, Assignee respectfully traverses the rejection to claim 6 and requests that Examiner withdraw it.

Claim 7 was rejected under 35 U.S.C. § 103(a) as being obvious from the combination of Wise in view of Kim. Claim 7 recites, among other limitations, "wherein the logic determines that the parameters are invalid if the control register indicates that the type of picture is a B-picture and less than two of the one or more bits are in the

particular state". Examiner has indicated that the foregoing is taught at Wise-pg. 51 0682 Table A.3.2; Pg. 13, 0160, 0165; pg. 18, 0220-0221; pg. 117 1595; Kim - Abstract; Col. 1 Lines 44-57; Fig. 1; Fig. 4; Fig. 6; Col. 6 Lines 8-12.

For the reasons indicated above, Kim - Abstract; Col. 1 Lines 44-57; Fig. 1; Fig. 4; Fig. 6; Col. 6 Lines 8-12 does not teach the limitations of claims 1 (as now amended), 4, 5, and 6. Furthermore, clearly the foregoing as well as Wise, Pg. 13, 0160, 0165; pg. 18, 0220-0221; pg. 117 1595, do not even mention the conditions "that the type of picture is a B-picture", "less than two of the one or more bits are in the particular state". Accordingly, Assignee respectfully traverses the rejection to claim 7 and requests that Examiner withdraw it.

Claim 8 is amended to recite, among other limitations, "wherein determining the validity of the parameters is based on the picture type indicator and the number of motion vectors received". Examiner has indicated that Wise does not specifically teach determining the validity of the parameters is based on the picture type indicator and the number of motion vectors received. Office Action at 5. Accordingly, Assignee respectfully requests that Examiner withdraw the rejection to claims 8 and 9 under 35 U.S.C. § 102(a).

Examiner has indicated that Kim teaches determining the validity of the parameters is based on the picture type indicator and the number of motion vectors received. [Col. 1 Lines 44-57]".

Assignee respectfully submits that the mere teaching of "A maximum of 4 MVs can be obtained per macroblock" does not teach that the "wherein determining the validity of the

parameters is based on the picture type indicator and the number of motion vectors received by the input". It is first noted that Kim does not even teach even teach "determining the validity of the parameters". Moreover, even if Kim's statement that "A maximum of 4 MVs can be obtained per macroblock" is construed to determine "whether parameters received by the input are valid" it is not "based on the picture type indicator". Accordingly, Assignee respectfully traverses the rejection to claim 10 as originally submitted, and requests that Examiner allow claim 8 as now amended, as well as dependent claims 9, 11, and 12.

Claim 13 was rejected under 35 U.S.C. § 103(a) as being obvious from the combination of Wise in view of Kim. Claim 13 is amended to recite, among other limitations "wherein the motion vector address computer determines whether the parameters received by the input are valid based on the picture type indicator and the number of motion vectors received by the input".

Examiner has indicated that the foregoing is taught by Kim – Col. 1, Lines 44-57. Office Action at 7. Assignee respectfully submits that the mere teaching of "A maximum of 4 MVs can be obtained per macroblock" does not teach that the "motion vector address computer determines whether the parameters received by the input are valid based on the picture type indicator and the number of motion vectors received by the input". It is first noted that Kim does not even teach even teach determining "whether the parameters received by the input are valid". Moreover, even if Kim's statement that "A maximum of 4 MVs can be obtained per macroblock" is construed to determine "whether parameters received by the input are valid" it is not "based on the

picture type indicator". Accordingly, Assignee respectfully traverses the rejection to claim 16 as originally submitted, and requests that Examiner allow claim 13 as now amended, as well as dependent claims 14, 15, and 17-20.

CONCLUSION

For at least the foregoing reasons, Assignee respectfully submits that each of the pending claims are allowable and Examiner is respectfully requested to pass this case to issuance. The Commissioner is hereby authorized to charge additional fees or credit overpayments to the deposit account of McAndrews, Held & Malloy, Account No. 13-0017.

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Respectfully submitted,

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